

COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC207	LOGIC CIRCUIT DESIGN	3-0-0-3	2016
Prerequisite: Nil			
Course objectives:			
<ul style="list-style-type: none"> To work with a positional number systems and numeric representations To introduce basic postulates of Boolean algebra and show the correlation between Boolean expression To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits To study the fundamentals of HDL To design and implement combinational circuits using basic programmable blocks To design and implement synchronous sequential circuits 			
Syllabus:			
Positional Number Systems, Boolean algebra, Combinational Logic, HDL concepts ,Digital ICs, Programmable Logic Devices, Sequential Logic, Sequential Circuits			
Expected outcome:			
The student should able to:			
1. Compare various positional number systems and binary codes			
2. Apply Boolean algebra in logic circuit design			
3. Design combinational and sequential circuits			
4. Design and implement digital systems using basic programmable blocks			
5. Formulate various digital systems using HDL			
Text Books:			
1. Donald D Givone, Digital Principles and Design, Tata McGraw Hill, 2003			
2. John F Wakerly, Digital Design Principles and Practices, Pearson Prentice Hall, 2007			
References:			
1.Ronald J Tocci, Digital Systems, Pearson Education, 11 th edition,2010			
2.Thomas L Floyd, Digital Fundamentals, Pearson Education, 8 th edition			
2009 3.Moris Mano, Digital Design, Prentice Hall of India, 3 rd edition, 2002			
4.John M Yarbrough, Digital Logic Applications and Design, Cenage learning, 2009			
5.David Money Harris, Sarah L Harris, Digital Design and Computer Architecture, Morgan Kaufmann – Elsevier, 2009			
Course Plan			
Module	Course content (42 hrs)	Hours	Sem. Exam Marks
I	Number systems- decimal, binary, octal, hexa decimal, base conversion	2	15
	1's and 2's complement, signed number representation Binary arithmetic, binary subtraction using 2's complement	2	
	Binary codes (grey, BCD and Excess-3), Error detection and correcting codes : Parity(odd, even), Hamming code (7,4), Alphanumeric codes : ASCII	2	
II	Logic expressions, Boolean laws, Duality, De Morgan's law, Logic functions and gates	2	15
	Canonical forms: SOP, POS, Realisation of logic expressions using K-	2	

	map (2,3,4 variables)			
	Design of combinational circuits – adder, subtractor, 4 bit adder/subtractor, BCD adder, MUX, DEMUX, Decoder,BCD to 7 segment decoder, Encoder, Priority encoder, Comparator (2/3 bits)	4		
FIRST INTERNAL EXAM				
III	Introduction to HDL : Logic descriptions using HDL, basics of modeling (only for assignments)	2	0	
	Logic families and its characteristics: Logic levels, propagation delay, fan in, fan out, noise immunity , power dissipation, TTL subfamilies	1		15
	NAND in TTL (totem pole, open collector and tri-state), CMOS:NAND, NOR, and NOT in CMOS, Comparison of logic families (TTL,ECL,CMOS) in terms of fan-in, fan-out, supply voltage, propagation delay, logic voltage and current levels, power dissipation and noise margin	2		
	Programmable Logic devices - ROM, PLA, PAL, implementation of simple circuits using PLA	2		
IV	Sequential circuits - latch, flip flop (SR, JK, T, D), master slave JK FF, conversion of FFs, excitation table and characteristic equations	3	15	
	Asynchronous and synchronous counter design, mod N counters, random sequence generator	5		
SECOND INTERNAL EXAM				
V	Shift Registers - SIPO, SISO, PISO, PIPO, Shift registers with parallel LOAD/SHIFT Shift register counter - Ring Counter and Johnson Counter	3	20	
	Mealy and Moore models, state machine ,notations, state diagram, state table, transition table, excitation table, state equations	3		
VI	Construction of state diagram – up down counter, sequence detector	3	20	
	Synchronous sequential circuit design - State equivalence	2		
	State reduction – equivalence classes, implication chart	2		
END SEMESTER EXAM				

Assignments:

1. Simple combinational circuit design using MUX, DEMUX, PLA & PAL
2. HDL simulation of circuits like simple ALU, up-down counter, linear feedback shift register, sequence generator

Question Paper Pattern (End Sem Exam)

Maximum Marks: 100

Time : 3 hours

The question paper shall consist of three parts. Part A covers modules I and II, Part B covers modules III and IV, and Part C covers modules V and VI. Each part has three questions uniformly covering the two modules and each question can have maximum four subdivisions. In each part, any two questions are to be answered. Mark pattern is according to the syllabus with maximum 50 % for theory, derivation, proof and 50% for logical/numerical problems.