

COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC304	VLSI	3-0-0-3	2016
Prerequisite: EC203 Solid State Devices, EC204 Analog Integrated Circuit.			
Course objectives: <ul style="list-style-type: none"><li>To give the knowledge about IC Fabrication Techniques</li><li>To impart the skill of analysis and design of MOSFET and CMOS logic circuits.</li></ul>			
Syllabus: IC Fabrication Technology, CMOS IC Fabrication Sequence, CMOS inverters, Design rules, Static CMOS Design, Dynamic CMOS circuits, Pass transistor, Read Only Memory, Random Access Memory, Sense amplifiers, Adders, multipliers, Testing of VLSI circuits.			
Expected outcome: The students will be able to design and analyse various MOSFET and CMOS logic circuits.			
Text Books: <ul style="list-style-type: none"><li>John P Uyemura, Introduction to VLSI Circuits and Systems, Wiley India, 2006</li><li>S.M. SZE, VLSI Technology, 2/e, Indian Edition, McGraw-Hill,2003</li></ul>			
References: <ul style="list-style-type: none"><li>Jan M.Rabaey, Digital Integrated Circuits- A Design Perspective, Prentice Hall, Second Edition, 2005.</li><li>Neil H.E. Weste, Kamran Eshraghian, Principles of CMOS VLSI Design- A Systems Perspective, Second Edition. Pearson Publication, 2005</li><li>Razavi - Design of Analog CMOS Integrated Circuits,1e, McGraw Hill Education India Education, New Delhi, 2003.</li><li>Sung –Mo Kang &amp; Yusuf Leblebici, CMOS Digital Integrated Circuits- Analysis &amp; Design, McGraw-Hill, Third Ed., 2003.</li><li>Yuan Taur &amp; Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2008</li></ul>			
Course Plan			
Module	Course content	Hours	End Sem. Exam Marks
I	Material Preparation- Purification, Crystal growth (CZ and FZ process), wafer preparation	4	15
	Thermal Oxidation- Growth mechanisms, Dry and Wet oxidation, Deal Grove model.		
	Diffusion- Fick’s Laws, Diffusion with constant surface concentration and from a constant source, diffusion techniques.	3	
	Ion implantation-Technique, Range Theory, annealing.		
II	Epitaxy : Vapour phase epitaxy and molecular beam epitaxy	4	15
	Lithography- Photo lithographic sequence, Electron Beam Lithography, Etching and metal deposition		
	Methods of isolation Circuit component fabrication: transistor, diodes, resistors, capacitors, N-well CMOS IC Fabrication Sequence	3	
FIRST INTERNAL EXAM			
III	CMOS inverters- DC characteristics, switching characteristics, power dissipation	4	15

	<b>Layout Design rules</b> , Stick Diagram and layout of CMOS Inverter, two input NAND and NOR gates	4	
<b>IV</b>	<b>MOSFET Logic Design</b> -Pass transistor logic, Complementary pass transistor logic and transmission gate logic , realization of functions	6	<b>15</b>
<b>SECOND INTERNAL EXAM</b>			
<b>V</b>	<b>Read Only Memory</b> -4x4 MOS ROM Cell Arrays(OR,NOR,NAND) <b>Random Access Memory</b> –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell	4	<b>20</b>
	<b>Sense amplifiers</b> –Differential Voltage Sensing Amplifiers Introduction to PLDs and FPGAs, Design of PLAs.	3	
<b>VI</b>	<b>Adders</b> - Static adder, Carry-By pass adder, Linear Carry-Select adder, Square- root carry- select adder <b>Multipliers</b> -Array multiplier	4	<b>20</b>
<b>END SEMESTER EXAM</b>			

### Question Paper Pattern ( End Semester Exam)

**Maximum Marks : 100**

**Time : 3 hours**

The question paper shall consist of three parts. Part A covers modules I and II, Part B covers modules III and IV, and Part C covers modules V and VI. Each part has three questions uniformly covering the two modules and each question can have maximum four subdivisions. In each part, any two questions are to be answered. Mark patterns are as per the syllabus with 70% for theory and 30% for logical/numerical problems, derivation and proof.

