COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC464	LOW POWER VLSI	3-0-0 -3	2016

Prerequisite: EC 304 VLSI, EC308 Embedded Systems

Course objectives:

- To identify the power dissipation mechanisms in various MOS logic styles
- To familiarize suitable techniques to reduce power dissipation

Syllabus:

Physics of Power dissipation in MOSFET devices, Sources of power dissipation in CMOS, Circuit techniques for leakage power reduction, Design and test of low voltage CMOS, Non clocked circuit design style, Adiabatic switching.

Expected outcome:

The students will be able to:

i. Identify the sources of power dissipation in digital IC systems.
ii. Understand the impact of power on system performance and reliability
iii. Understand leakage sources and reduction techniques
iv. Recognise advanced issues in VLSI systems, specific to the deep-submicron silicon technologies
v. Identify the mechanisms of power dissipation in CMOS integrated circuits

Text Books:

1. Gray Yeap, Practical low power digital VLSI design, Springer, 1998
2. Kaushik Roy, Sharat C Prasad, Low power CMOS VLSI circuit design, Wiley India, 2000

References:

1. Abdellatif Bellaouar, Mohamed I Elmasry, Low power digital VLSI design, Kluwer Academic, 1995
2. Anatha P Chandrakasan, Robert W Brodersen, Low power digital CMOS Design, Kluwer Academic, 1995
3. Christian Piguet, Low power CMOS circuits, Taylor & Francis, 2006
4. Kiat Seng Yeo, Kaushik Roy, Low voltage, low power VLSI sub systems, Tata McGraw Hill, 2004

Course Plan

Module	Course contents	Hours	End Sem. Exam Marks
I	**Physics of Power dissipation in MOSFET devices** MIS structure, Need for low power circuit design	2	15%
	Threshold voltage, body effects,	1	
	Short channel effects-surface scattering, punch through, velocity saturation, impact ionization	2	
	Hot electron effects, drain induced barrier lowering, narrow width effects	2	
II	**Sources of power dissipation in CMOS**-Switching power dissipation,	2	15%
	Short circuit power dissipation, glitching power dissipation	2	
	Leakage power dissipation, Transistor leakage mechanisms of	3	

	deep submicron transistors		
FIRST INTERNAL EXAM			
III	**Circuit techniques for leakage power reduction** – standby leakage control using transistor stacks	2	**15%**
	multiple V_{th} techniques, Dynamic V_{th} techniques	2	
	supply voltage scaling techniques, Deep submicron devices design issues	2	
	Minimizing short channel effect	2	
IV	**Design and test of low voltage CMOS** – Circuit design style- clocked design style- Basic concept	2	**15%**
	Domino logic (domino NAND gate)	1	
	Differential Current Switch Logic.	2	
SECOND INTERNAL EXAM			
V	**Non clocked circuit design style**-fully complementary logic	2	**20%**
	NMOS and pseudo –NMOS logic	2	
	differential cascade voltage switch logic(DCVS),	2	
	pass transistor logic	2	
VI	**Adiabatic switching** – Adiabatic charging, adiabatic amplification	2	**20%**
	One stage and two stage adiabatic buffer	2	
	fully adiabatic system	1	
	Adiabatic logic gates, pulsed power supplies	2	
END SEMESTER EXAM			

Question Paper Pattern

The question paper shall consist of three parts. Part A covers modules I and II, Part B covers modules III and IV, and Part C covers modules V and VI. Each part has three questions uniformly covering the two modules and each question can have maximum four subdivisions. In each part, any two questions are to be answered. Mark patterns are as per the syllabus with 60% for theory and 40% for logical/numerical problems, derivation and proof.