COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC462	MIXED SIGNAL CIRCUIT DESIGN	3-0-0 -3	2016

Prerequisite: EC 304 VLSI, EC308 Embedded Systems

Course objectives:

- To give the knowledge about various analog and digital CMOS circuits
- To impart the skill in analysis and design of analog and digital CMOS circuits.

Syllabus:

CMOS Amplifiers**:** CS,CG,CD stages, Cascoded stages, Folded cascode Amplifier, MOS Current Mirror, MOSFET cascode current mirror, Differential Amplifiers, MOS telescopic cascode amplifier,CMOS OP AMPS, Design of classical Two Stage OP AMP, Comparator, Band gap References, Phase Locked Loop, Dynamic analog circuits, Data Converters, Switched Capacitor Circuits, Data Converters- Specifications, DAC, ADC Architecture

Expected outcome:

The students will be able to design and analyse various analog and digital CMOS circuits.

Text Books:

1. Phillip E. Allen, Douglas R. Holbery, CMOS Analog Circuit Design, Oxford, 2004.
2. Razavi B., Fundamentals of Microelectronics, Wiley student Edition2014.

References:

1. Baker, Li, Boyce, CMOS: Circuits Design, Layout and Simulation, Prentice Hall India, 2000
2. Razavi B., Design of Analog CMOS Integrated Circuits, Mc Graw Hill, 2001.

Course Plan

Module	Course contents	Hours	End Sem. Exam Marks
I	**CMOS Amplifiers-** Common Source with diode connected loads and current source load, CS stage with source degeneration, CG stage and Source Follower (Only Voltage Gain and Output impedance of circuits)	4	**15%**
	Cascoded stages - Cascoded amplifier, Cascoded amplifier with cascoded loads , Folded cascode Amplifier	4	
II	**MOS Current Mirror**- Basic circuit, PMOS and NMOS current mirrors Current mirror copying circuits, MOSFET cascode current mirror circuits	3	**15%**
	Differential Amplifiers-Differential Amplifier with MOS current source Load, with cascaded load and with current mirror load, MOS telescopic cascode amplifier. (Only Voltage Gain and Output impedance of circuits)	4	
FIRST INTERNAL EXAM			
III	**CMOS OP AMPS-** Two Stage Operational Amplifiers - Frequency compensation of OPAMPS - miller compensation**,**	3	**15%**

	Design of classical Two Stage OP AMP		
	Comparator- Characterization of a comparator-static and dynamic, A Two stage open loop comparator (analysis not required)	3	
IV	**Band gap References-** Supply Independent Biasing, Temperature independent references –band gap reference	5	**15%**
	Phase Locked Loop – Simple PLL ,Basic PLL Topology, Charge Pump PLL, Basic Charge Pump PLL	3	
SECOND INTERNAL EXAM			
V	**Dynamic analog circuits** – charge injection and capacitive feed through in MOS switch, Reduction technique	3	**20%**
	Switched Capacitor Circuits- sample and hold circuits, Switched Capacitor Integrator, Ladder filters	3	
VI	**Data Converters-** DAC Specifications-DNL, INL, latency, SNR, Dynamic Range ADC Specifications-Quantization error, Aliasing, SNR, Aperture error	4	**20%**
	DAC Architecture - Resistor String, Charge Scaling and Pipeline types. **ADC Architecture-** Flash and Pipe line types	3	
END SEMESTER EXAM			

Question Paper Pattern

The question paper shall consist of three parts. Part A covers modules I and II, Part B covers modules III and IV, and Part C covers modules V and VI. Each part has three questions uniformly covering the two modules and each question can have maximum four subdivisions. In each part, any two questions are to be answered. Mark patterns are as per the syllabus with 60% for theory and 40% for logical/numerical problems, derivation and proof.